

What is claimed is:

1 1. A method for identifying defects in an integrated circuit, comprising the steps of:
2 measuring a current signature delta value of a device under test; and
3 comparing the current signature delta value to a threshold current signature delta value to
4 determine whether the current signature delta value is greater than the threshold current signature
5 delta value.

1 2. The method according to claim 1, further comprising the step of generating the
2 threshold current signature delta value for a statistically valid number of acceptable integrated
 circuits.

1 3. The method according to claim 2, wherein the step of generating the threshold
2 current signature delta value that correlates to the acceptable integrated circuit further comprises
3 the steps of:

4 applying a set of vectors to a statistically valid number of acceptable integrated circuits;

5 formulating a threshold base current signature for the statistically valid number of
6 acceptable integrated circuits;

7 administering a voltage stress for a time period to each of the statistically valid number of
8 acceptable integrated circuits;

9 applying the set of vectors to the statistically valid number of acceptable integrated
10 circuits;

11 formulating a threshold post-stress current signature for the statistically valid number of
12 acceptable integrated circuits;

13 comparing the threshold base current signature for the statistically valid number of
14 acceptable integrated circuits to the threshold post-stress current signatures for the statistically
15 valid number of acceptable integrated circuits to determine a threshold current signature delta
16 value corresponding to an acceptable integrated circuit.

1 4. The method according to claim 1, further comprising the step of generating the
2 threshold current signature delta value using a computer.

1 5. The method according to claim 3, wherein the step of measuring the current
2 signature delta value of the device under test further comprises the steps of:
3 applying a set of vectors to the device under test and formulating a base current signature
4 for the device under test;
5 administering a voltage stress to the device under test for a time period;
6 applying the set of vectors to the device under test and formulating a post-voltage stress
7 current signature for the device under test; and
8 determining the current signature delta value for the device under test.

1 6. The method according to claim 4, wherein the step of measuring the current
2 signature delta value of the device under test further comprises the steps of:
3 applying a set of vectors to the device under test and formulating a base current signature
4 for the device under test;
5 administering a voltage stress to the device under test for a time period;
6 applying the set of vectors to the device under test and formulating a post-voltage stress
7 current signature for the device under test; and
8 determining the current signature delta value for the device under test.

1 7. The method according to claim 5, further comprising the step of:
2 comparing the post-voltage stress current signature of the device under test to the
3 threshold post-voltage stress current signature to determine whether the post-voltage stress
4 current signature of the device under test is greater.

1 8. The method according to claim 6, further comprising the step of:
2 comparing the post-voltage stress current signature of the device under test to the
3 threshold post-voltage stress current signature to determine whether the post-voltage stress
4 current signature of the device under test is greater.

1 9. The method according to claim 7, wherein the threshold current signature delta
2 value is equivalent to a largest difference between the threshold post-voltage stress current
3 signature and the threshold base current signature for the statistically valid number of acceptable
4 integrated circuits.

1 10. The method according to claim 8, wherein the current signature delta value for the
2 device under test is a difference between the post-voltage stress current signature and the base
3 current signature of the device under test.

1 11. The method according to claim 9, wherein the current signature delta value for the
2 device under test is a difference between the post-voltage stress current signature and the base
3 current signature of the device under test.

1 12. The method according to claim 11, wherein said formulating the threshold base
2 current signature for the statistically valid number of acceptable integrated circuits further
3 comprises the steps of:
4 measuring a base current response for each vector of a set of measured vectors from the
5 set of vectors applied to each of the statistically valid number of acceptable integrated circuits;
6 determining the lowest base current response for each vector as applied across each of the
7 statistically valid number of acceptable integrated circuits; and
8 plotting the lowest base current responses for the set of vectors into the threshold base
9 current signature.

1 13. The method according to claim 12, wherein said formulating the threshold post-
2 voltage stress current signature for the statistically valid number of acceptable integrated circuits
3 further comprises the steps of:

4 measuring a post-voltage stress current response for each vector of a set of measured
5 vectors from the set of vectors applied across each of the statistically valid number of acceptable
6 integrated circuits;

7 determining the highest post-voltage stress current response for each vector as applied
8 across each of the experimental ICs; and

9 plotting the highest post-voltage stress current responses for the set of vectors into the
10 threshold post-voltage stress current signature.

1 14. The method according to claim 13, wherein said formulating the base current
2 signature for the device under test comprises the step of measuring a current response for each
3 vector of the set of measured vectors applied to the device under test and plotting the current
4 response for each vector of the set of measured vectors into the base current signature for the
5 device under test.

1 15. The method according to claim 14, wherein said formulating the post-voltage
2 stress current signature for the device under test comprises the step of measuring a post-voltage
3 stress current response for each vector of the set of measured vectors applied to the device under
4 test after said administering the voltage stress for the time period, and plotting the post-voltage
5 stress current response for each vector of into the post-voltage stress current signature for the
6 device under test.

1 16. The method according to claim 15, wherein the statistically valid number of
2 acceptable integrated circuits must have the same architecture as the device under test.

1 17. The method according to claim 16, wherein the statistically valid number of
2 acceptable integrated circuits must be produced using the same semiconductor wafer process
3 technology as the device under test.

1 18. The method according to claim 17, wherein the threshold base current signature
2 and the threshold post-voltage stress current signature for the statistically valid number of
3 acceptable integrated circuits are threshold base quiescent current signatures and threshold post-
4 stress quiescent current signatures.

1 19. The method according to claim 18, wherein the threshold base current signature
2 and the threshold post-voltage stress current signature for the device under test is a threshold
3 base quiescent current signature and a threshold post-voltage stress quiescent current signature.

1 20. The method according to claim 19, wherein after said applying the set of vectors
2 to the statistically valid number of acceptable integrated circuits and prior to said formulating the
3 threshold base quiescent current signature for the statistically valid number of acceptable
4 integrated circuits, each of the statistically valid number of acceptable integrated circuits are
5 allowed to reach a steady state before the current measurement is recorded.

1 21. The method according to claim 20, wherein after said administering the voltage
2 stress, after said applying the set of vectors to the statistically valid number of acceptable
3 integrated circuits and prior to said formulating the threshold post-voltage stress quiescent
4 current signature for the statistically valid number of acceptable integrated circuits, the
5 statistically valid number of acceptable integrated circuits are allowed to reach a steady state
6 before the current measurement is recorded.

1 22. The method according to claim 21, wherein after said applying the set of vectors
2 to the device under test and prior to said formulating the base current signature for the device

3 under test, the device under test is be allowed to reach steady state before each current
4 measurement is recorded.

1 23. The method according to claim 22, wherein after said administering the voltage
2 stress, after said applying the set of vectors to the device under test and prior to said formulating
3 the post-voltage stress current signature for the device under test, the device under test is allowed
4 to reach steady state before each current measurement is recorded.

1 24. The method according to claim 17, wherein the base current signatures and the
2 post-stress current signatures for each of the statistically valid number of acceptable integrated
3 circuits are base transient current signatures and post-stress transient current signatures.

1 25. The method according to claim 24, wherein the base current signature and the
2 post-voltage stress current signature for the device under test is a base transient current signature
3 and a post-stress transient current signature.

1 26. The method according to claim 23, wherein the set of vectors is generated using
2 an automatic test generation program.

1 27. The method according to claim 26, wherein said applying a set of vectors to the
2 device under test and the statistically valid number of acceptable integrated circuits is performed
3 using a VLSI test system.

1 28. The method according to claim 27, wherein said measuring the current signature
2 delta value of the device under test and the statistically valid number of acceptable integrated
3 circuits is performed using the VLSI test system.

1 29. The method according to claim 28, wherein the set of vectors comprises less than
2 one hundred vectors.

1 30. The method according to claim 29, wherein the set of vectors comprises vectors
2 associated with a high fault coverage for the device under test.

1 31. The method according to claim 30, wherein the set of vectors comprises vectors
2 associated with low current off-states for the device under test.

1 32. The method according to claim 31, wherein the time period for said administering
2 the voltage stress to the statistically valid number of acceptable integrated circuits and to the
3 device under test is equivalent to the minimum amount of time that the voltage stress can be
4 administered to an acceptable integrated circuit in which the acceptable integrated circuit remains
5 acceptable.

1 33. An apparatus for identifying defects in an integrated circuit, comprising:
2 a generator for generating a set of vectors for applying to a device under test;
3 a measurer for measuring a current signature delta value of the device under test; and
4 a comparing means for comparing the current signature delta value to an experimental
5 threshold current signature delta value to determine whether the current signature delta value is
6 greater than the threshold current signature delta value.

1 34. The apparatus according to claim 33, wherein the measurer measures the
2 experimental threshold current signature delta value for the statistically valid number of
3 acceptable integrated circuits by:
4 applying a set of vectors to the statistically valid number of acceptable integrated circuits;
5 formulating a threshold base current signature for the statistically valid number of
6 acceptable integrated circuits from the set of measured vectors;

7 administering a voltage stress for a time period to the statistically valid number of
8 acceptable integrated circuits;
9 applying the set of vectors to the statistically valid number of acceptable integrated
10 circuits;
11 formulating a threshold post-stress current signature for the statistically valid number of
12 acceptable integrated circuits from the set of measured vectors; and
13 comparing the threshold base current signature for the statistically valid number of
14 acceptable integrated circuits to the threshold post-stress current signatures for the statistically
15 valid number of acceptable integrated circuits to determine a threshold current signature delta
16 value corresponding to an acceptable integrated circuit.

1 35. The apparatus according to claim 33, further comprising a computer for
2 computing the experimental threshold current signature delta value.

1 36. The apparatus according to claim 33, wherein the generator generates a set of
2 measured vectors from the set of vectors for applying to the device under test.

1 37. The apparatus according to claim 35, wherein the measurer measures the current
2 signature delta value of the device under test by:
3 applying a set of vectors to the device under test;
4 formulating a base current signature for the device under test from the set of measured
5 vectors;
6 administering a voltage stress for a time period to the device under test;
7 applying the set of vectors to the device under test;
8 formulating a threshold post-stress current signature for the device under test from the set
9 of measured vectors;

10 comparing the base current signature for the device under test to the post-stress current
11 signatures for the device under test to determine a the current signature delta value for the device
12 under test.

1 38. The apparatus according to claim 36, wherein the measurer measures the current
2 signature delta value of the device under test by:
3 applying a set of vectors to the device under test;
4 formulating a base current signature for the device under test from the set of measured
5 vectors;
6 administering a voltage stress for a time period to the device under test;
7 applying the set of vectors to the device under test;
8 formulating a threshold post-stress current signature for the device under test from the set
9 of measured vectors; and
10 comparing the base current signature for the device under test to the post-stress current
11 signatures for the device under test to determine a the current signature delta value for the device
12 under test.

1 39. The apparatus according to claim 37, wherein the threshold current signature delta
2 value generated by the generator is equivalent to a largest difference between the post-voltage
3 stress current signature and the base current signature of the statistically valid number of
4 acceptable integrated circuits.

1 40. The apparatus according to claim 38, wherein the threshold current signature delta
2 value generated by the generator is equivalent to a largest difference between the post-voltage
3 stress current signature and the base current signature of the statistically valid number of
4 acceptable integrated circuits.

1 41. The apparatus according to claim 39, wherein the current signature delta value for
2 the device under test is a difference between the post-voltage stress current signature and the base
3 current signature of the device under test.

1 42. The apparatus according to claim 41, wherein the generator generates the set of
2 vectors for applying to a statistically valid number of acceptable integrated circuits; and the
3 measurer measures the experimental threshold current signature delta value of the statistically
4 valid number of acceptable integrated circuits.